IN THE CLAIMS

This version of the claims replaces and supercedes all prior versions of the claims.

1. (Currently Amended) A processor having a plurality of processor functions for executing each of a plurality of instruction sets, comprising:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction ~~that is~~ not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to one of

said system instruction decoded by said system instruction decoder, and

a prescribed interrupt signal.

2. (Canceled)

3. (Original) The processor according to claim 1, wherein at least two of the plurality of processor functions share hardware resources.

4. (Original) The processor according to claim 1, wherein at least two of the plurality of instruction sets include a common instruction, and a plurality of processor functions corresponding to said at least two instruction sets share an instruction set decoder for decoding the common instruction.

5. (Original) The processor according to claim 1, wherein the system instruction includes at least one instruction that sets power-supply voltage and operating speed at which the processor operates.

6. (Original) The processor according to claim 1, further comprising a storage unit for storing processing control data corresponding to each instruction included in the plurality of instruction sets;

wherein on the basis of an entered instruction and information regarding a selected processor function, an address that corresponds to the entered instruction is generated and processing control data corresponding to the entered instruction is read out of said storage unit.

7. (Original) The processor according to claim 1, wherein at least two processor functions among the plurality thereof have a common instruction set.

8. (Original) The processor according to claim 1, wherein at least one processor function among the plurality thereof undergoes pipeline control in which number of stages thereof is set variably, and the number of stages in the pipeline control is set in response to a predetermined system instruction.

9. (Original) A processor having a pipeline control architecture, said processor comprising:

a unit for receiving a stage-number setting instruction; and

a unit for setting variably the number of stages in the pipeline control in response to the received stage-number setting instruction.

10. (Original) A system LSI circuit having the processor set forth in claim 1.

11. (Original) A system LSI circuit having a plurality of the processors set forth in claim 1.

12. (Original) The system LSI circuit according to claim 11, wherein the plurality of processors operate based upon either a first pattern in which all processors operate according to the same instruction set, or a second pattern in which at least one processor operates according to an instruction set that is different from those of the other processors.

13-19. (Cancelled)

20. (Withdrawn) A computer-readable recording medium on which is recorded a program for causing a computer to execute designing a system LSI circuit having a plurality of processor functions for executing a plurality of instruction sets, said program comprising:

(a) dividing system LSI circuit design specifications into hardware design and software design at a function designing stage;

(b) receiving, in hardware design, as hardware information, hardware configurations corresponding to respective ones of the plurality of processors, and the system instruction and the plurality of instruction sets described at an algorithm level; and

(c) performing behavioral synthesis using the hardware information, wherein said processor includes:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to the system instruction decoded by said system instruction decoder.

21. (Original) A processor apparatus comprising:

an instruction fetch register for storing an instruction fetched;

a plurality of instruction decoders, each receiving and decoding an instruction of an instruction set associated with said instruction decoder;

a plurality of instruction execution controllers, each being provided in association with the corresponding instruction decoder, for receiving a decoded result of the instruction by the corresponding instruction decoder for controlling the execution of the instruction;

an instruction set change over unit for selecting at least one among the plurality of instruction decoders and for supplying an instruction output from said instruction fetch register to the selected instruction decoder;

a system instruction decoder receiving a predetermined system instruction from instruction fetch register for decoding the predetermined system instruction; and

a system instruction execution controller receiving the decoded result from said system instruction decoder; said system instruction execution controller controlling said instruction set change over unit to change over the selection of the plurality of instruction decoders, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction specifying the instruction set to be used among a plurality of instruction sets.

22. (Original) The processor apparatus according to claim 21, wherein said system instruction execution controller performs control to dynamically change over the number of stages in a pipeline from an instruction fetch stage to an instruction execution stage for an instruction set being used, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction that specifies the number of pipeline stages for the instruction set.

23. (Previously Presented) A processor that performs a first instruction set and a second instruction set, comprising:

a first processing unit that executes processing based on only a first decoded result,

among a first decoded result and a second decoded result, the first decoded result being a decoded signal of an instruction included in the first instruction set, the second decoded result being a decoded signal of an instruction included in the second instruction set; and

a common processor unit that executes processing based on both the first and second decoded results.

24. (Previously Presented) The processor according to claim 23, further comprising:

a first decoder that generates the first decoded result by decoding the instruction included in the first instruction set; and

a second decoder that generates the second decoded result by decoding the instruction included in the second instruction set.

25. (Previously Presented) The processor according to claim 24, further comprising:

a second processing unit that executes procession based on only the second decoded result among the first and second decoded results.

26. (Previously Presented) The processor according to claim 23, further comprising:

a common instruction set decoder that decodes a common instruction included commonly in the first and second instruction sets.

27. (Currently Amended) The processor according to claim 24, further comprising:

a pipeline stage that is provided between the first decoder and the first processing unit.

28. (Currently Amended) The processor according to claim 25, further comprising:

a first pipeline stage provided between the first decoder and the first processing unit; and

a second pipeline stage provided between the second decoder and the second processing unit.

29. (Previously Presented) The processor according to claim 28, wherein said first pipeline has a different number from said second pipeline.

30. (Previously Presented) The processor according to claim 27, wherein said stage number of the pipeline is variable.

31. (Previously Presented) The processor according to claim 28, wherein the stage number of the first and second pipelines are variable.

32. (Previously Presented) The processor according to claim 24, further comprising a system instruction decoder that decodes a system instruction which selects use of any one of the first and second decoders.

33. (Previously Presented) The processor according to claim 32, wherein said system instruction decoder is provided separate from the first and second decoders.

34. (Previously Presented) The processor according to claim 24, wherein any one of the first and second decoders is selected for use in response to an interrupt signal.

35. (Previously Presented) The processor according to claim 32, wherein said system instruction includes at least one of instructions for setting power voltage and/or operating rate at which the processor operates.

36. (Previously Presented) The processor according to claim 23, further comprising:

a memory that stores both the first and second decoded results.

37. (Previously Presented) The processor according to claim 36, further comprising:

a second processing unit that executes processing based on only the second decoded result among the first and second decoded results.

38. (New) The processor according to claim 23, further comprising:

a first register file for the first processing unit, and

a common register file for the common processor unit.

39. (New) The processor according to claim 37, further comprising:

a first register file for the first processing unit,

a second register file for the second processing unit, and

a common register file for the common processor unit.

40. (New) The processor according to claim 23, further comprising:

a register file being specific to the first instruction set.